REMARKS

Claims 1-44 remain pending in the current Application. Claims 1-3, 12, 15-16, 21, 24-25, 30-32, and 35-43 have been amended. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Anticipation Rejection of Claims 1-14, 17-18, 21-23, and 30-35, 37-38, and 40-44

At page 2 of the Office Action, claims 1-14, 17-18, 21-23, and 30-35, 37-38, and 40-44 are rejected under 35 U.S.C. § 102(b) as being unpatentable over Yoshida et al. (US 5,475,853). Applicants wish to thank the Examiner for the telephone discussions held on Monday, December 17, 2007, regarding the above application in which the amendments to the claims made herein were discussed.

With respect to claim 1, Applicants have clarified claim 1 to recite processor circuitry for executing one or more instructions, where a first *single instruction* specifies *both* a size of data elements in the memory *and* a size of data elements in the at least one general purpose register, where the first single instruction specifies the size of the data elements in memory separate and independent from specifying the size of the data elements in the at least one general purpose register. Applicants submit that neither the L-format nor the E-format instructions, as relied upon by the Examiner, teach or suggest a *single instruction* in which *both* the size of data elements in the memory *and* a size of the data elements in the at least one general purpose instruction can be specified, separately and independently from each other. Below, Applicants are including the arguments previously made, for the Examiner's convenience.

In rejecting claim 1, the Examiner indicated, in the Office Action mailed Nov. 13, 2006, that this claim 1 limitation is disclosed by Yoshida at column 9, lines 28-36. Applicants respectfully disagreed, and noted that Yoshida as relied upon by the Examiner discloses a destination register (the general purpose register) having a predetermined data element size that is fixed at 32-bits (e.g. the L-format). In the Final Rejection mailed April 19, 2007, in response to the above argument, the Examiner states that "although Yoshida teaches that the

size of the destination operand located in the register is fixed, this teaching only applies to a singular type of instruction format type ('L-format' disclosed in column 9, lines 23-27)," and proceeds to indicate that Yoshida "also teaches information format types ('E-format' disclosed in column 10, lines 26-43) in which the sizes of the data elements are specified separately in both the memory and the general purpose registers." However, Applicant respectfully disagrees. The E-format instruction of Yoshida does not transfer data elements between the memory *and at least one general purpose register*. The E-format, as described in column 10, lines 26-32, and FIG. 9, is an instruction where a first operand (the source operand) is an *immediate value* provided within the instruction itself (field 256 represents the source operand value) and thus is not provided as a data element in at least one general purpose register. Furthermore, this first operand of the E-format is a *fixed* eight bit immediate (see, e.g., column 10, lines 27-28 and lines 36-37). The second operand (destination operand) of the E-format is in memory. Therefore, the E-format does not teach or suggest the ability to specify the size of a data element in a general purpose register. That is, the E-format does not include a transfer of data elements between memory *and at least one general purpose register*, and furthermore, the E-format does not even teach or suggest the ability to specify the size of the immediate value.

The Examiner also states that Yoshida discloses in column 10, lines 33-43, that the "E-format presupposes an operation between different sizes, and the source operand of eight bits is zero-extended or sign-extended in a manner of agreeing with the size of the destination operand." However, again, this does not teach or suggest the ability to specify the size of data elements in the memory separate and independent from specifying the size of the data elements in the at least one general purpose register. As discussed above, the immediate value is a *fixed* 8-bit value (and is also *not* a data element *in the at least one general purpose register*), therefore, even though the E-format may have an operation between *different* sizes, both the sizes are not able to be *separately and independently* specified, as claimed. Therefore, for at least these reasons, Applicant submits that claim 1 is patentable over Yoshida.

Claims 2-14, 17-18, and 21-23, which are rejected under section 102 based upon Yoshida, are also not anticipated by Yoshida by virtue of their dependency from claim 1. Therefore, for at least these additional reasons, Applicant respectfully requests withdrawal of the rejections of claims 2-14, 17-18, and 21-23. Note that Applicant has amended claims 2, 3, 12, and 21 to maintain consistency with the amendments made to claim 1.

Claim 30 recites executing one or more instructions, where a first *single instruction* specifies *both* a size of data elements in the memory *and* a size of data elements in the at least one general purpose register, where the first single instruction specifies the size of the data

elements in memory separate and independent from specifying the size of the data elements in the at least one general purpose register. that specify a size of data elements in the memory separate and independent from specifying size of data elements in a general purpose register. As argued with respect to claim 1, Yoshida does not disclose specifying a size of data elements in a general purpose register as recited in claim 20, but instead relies upon a predetermined fixed data element size or an immediate value having a fixed size. Therefore, Yoshida necessarily does not anticipate each and every element of claim 30 as recited. For at least this reason, the withdrawal of the rejection under section 102 of independent claim 30, based upon Yoshida, is respectfully requested.

Claims 31-35, 37-38, and 40 which are rejected under section 102 based upon Yoshida, are also not anticipated by Yoshida for the same reasoning as claim 30, at least by virtue of the dependency from claim 30. In addition, these claims disclose additional non-obvious limitations. For at least these reasons, withdrawal of the rejections of claims 31-35, 37-38, and 40 is respectfully requested. Note that Applicant has amended claims 31, 32, 35, 37, 38, and 40 to maintain consistency with the amendments made to claim 30.

Claim 41 recites a data processing system for executing one or more instructions, where a first single instruction includes control information that specifies both a size of data elements in the memory and a size of data elements stored in at least one storage location in the data processing system external to the memory, where the first single instruction specifies the size of the data elements stored in the memory separate and independent from specifying the size of the data elements stored in the at least one storage location in the data processing system external to memory. Yoshida does not disclose specifying a size of data elements in a location other than memory as recited in claim 41. Furthermore, many of the arguments provide above with respect to claim 1 also apply to claim 41. Therefore, Yoshida necessarily does not anticipate each and every element of claim 41 as recited. For at least this reason, the withdrawal of the rejection under section 102 of independent claim 41, based upon Yoshida, is respectfully requested.

Claims 42-44, which are rejected under section 102 based upon Yoshida, are also not anticipated by Yoshida at least by virtue of the dependency from claim 41. In addition, these claims disclose additional non-obvious limitations. For at least these reasons, withdrawal of the rejections of claims 42-44 is respectfully requested. Note that Applicants have amended claims 42 and 43 to maintain consistency with the amendments made to claim 41.

Obviousness Rejection of Claims 16, 19, 20, and 25-29

At page 11 of the Office Action, claims 16, 19, 20, and 25-29 have been rejected under 35 U.S.C. § 103(a) as being obvious over Yoshida et al. in view of Chung et al.(US 6,950,922). Each of these claims depend from claim 1. As previously argued, Yoshida does not disclose an instruction specifying a size of a data element in at least one of the general purpose registers as recited in claim 1. Similarly, Chung does not disclose instructions having this limitations recited in claim 1. Therefore, at least this reason, the combination of Yoshida and Chung does not disclose or suggest, alone or in combination, the recited elements of claims 16, 19, 20, and 25-29. Therefore withdrawal of the rejection of these claims under §103 is respectfully requested. Note that Applicant has amended claims 16 and 25 in order to maintain consistency with the amendments made to claim 1.

Obviousness Rejection of Claims 15, 24, 36. and 39

At page 14 of the Office Action, claims 15, 24, 36, and 39 are rejected under 35 U.S.C. § 103(a) as being obvious over Yoshida et al. in view of Paver et al.(US 6,950,922). Claims 15 and 24 depend from claim 1, claims 36 and 39 depend from claim 30. As previously argued, claims 1 and 30 do not disclose an instruction specifying the size of data elements as recited in claims 1 and 30. Furthermore, Paver does not disclose instructions as recited in claims 1 and 30. Therefore the combination of Yoshida in view of Paver does not disclose or suggest, alone or in combination, the recited elements of claims 15, 24, 36, and 39 as recited. Therefore, withdrawal of the rejection of these claims under §103 is respectfully requested. Note that Applicant has amended claims 15, 24, 36, and 39 in order to maintain consistency with the amendments to claims 1 and 30.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

By: /Joanna G. Chiu/
CHIU, JOANNA G.
Attorney of Record
Reg. No.: 43,629
Telephone: (512) 996-6839
Fax No.: (512) 996-6854